APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/662,832	09/15/2000	Timothy J. van Hook	1778.0100002	2552

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EXAMINER
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ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 49-64* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,49 and 52-64* is/are rejected.

7)☒ Claim(s) *50 and 51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/08/05*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

1.   Claims 1,49-64 remain for examination. This action include new comments and new rejections (to claims 1,52) regarding "101" by examiner based on newly updated version of the internal guidelines on 01/17/06. Therefore, in order to allow applicant a chance to respond , this is a non-final action. Response to applicant's remarks will follow. T.D. on 01/24,2002 has been entered. However, new T.D. may need to be filed in a continuation application. For purpose of examination, the Double Patenting rejections set forth in the last Office action are still pending. Claims 50,51 were objected pending on the "101" and ODP as set forth in the last offcie action.

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2.   Claims 1,49, 52 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

3.   As to claims 1, 49,52, the claims are reciting the loading , extracting ,and replicating (claim 1), writing (claim 49), selecting (claim 52) of the vectors from a memory into the vector registers. However, the vectors are not functional descriptive material. Although claim additionally recites the computer system (see preamble) and the SIMD (see preamble and last line of claim body), no physical transformation can be found into claim. The vector being replicated (or written claim 49, selected from the registers claim 52) into the third register is a transformation of data from one to another , and is not by itself sufficient for establishing the

eligibility of patent protection (e.g. see <u>Benson</u>, 409, U.S. 63, 175, USPQ 673). Furthermore,

no concrete , useful, tangible result can be found in the claim. For example, the SIMD is the

step taken to achieve a particular result, but it is not the final result. The focus for

determination of practical application is not on the steps taken to achieve a particular result are

useful, tangible, and concrete, but rather that the final result achieved by the claimed invention is

useful, tangible , and concrete (page 20 of the internal guidelines). Although claim 1 recites also

a computer system, no substantial practical application can be found in the claim. Moreover, the

evidence shows that the vectors might be directed to nonfunctional descriptive material (see the

static information stored in memory in applicant's specification page 8, lines 20-27) , no

functional descriptive material on a computer readable storage that provide necessary functional

and structural interrelationship in combination with the vectors can be found in claim.

Therefore, the claims do not constitute a statutory subject.

4.   The rejections are maintained and incorporated by reference the last office action on

08/08/05.

5.   The response on 12/08/05 by applicant has been fully considered but is not persuasive.

6.   In the remarks, applicant argued that :

a) SIMD is concrete, useful, and tangible;

b) the third register can be taught of as being transformed to data ready for SIMD processing;

c) neither Agarwal nor Cho teaches or suggests clamed features in claims 1,49,52;

d) applicant also presented claims 54-58.

7.   As to a) , the processing for SIMD is what intended to use for practical application, not

the practical application itself. No functional descriptive material on a computer readable

storage that provide necessary SIMD functional and structural interrelationship in combination

with the vectors can be found in claim.

8.   As to b) above, data ready for processing is not a final result. See the discussions in

paragraph 3 above.

9.   As to c) above, the amendment and reply on 01/24/02 has been considered by examiner.

In that applicant argued that Agarwal did not teach the starting byte of the first vector. Examiner

would like to point out that Agarwal taught the starting byte of the first vector (see 32 bit in the

first register , see the use of byte or word col. 15, lines 15-30, see also the aligned vector in col.

15, lines 31-67, col. 16, lines 1-14). Applicant also argued that Agarwal did not teach the

extracting the aligned vector from first register and second register beginning the starting byte ,

and the vectors were not taken from first and second registers and no alignment was taken place

in the step of writing a vector register in the array 238. The examiner would like to point out

that Agarwal taught extracting a first width vector (64 bit) from a first register beginning from

the first bit [higher/lower bit] continuing through a bit in second register (e.g. see the consecutive

single precision elements in col.15, lines 44-50). As to the alignment , see the aligned vectors in

col. 15, lines 31-67, col. 16, lines 1-14. The alignment had to be done in the writing in order

obtain a proper bit position. Applicant also argued the t applicant 's invention is direct to

elements in each vector register are selected by extracting a vector from the first vector register

and the second vector register. Cho disclosed an input selection circuit (310) for selecting a first

and a second data elements into a result register (see the selected output p in col. 13, lines 10-

25). The first and second data elements are the first and second registers, and the result register was the selected element. Cho did have extracting (see the selection) and alignment (see the rotate in fig.3). Applicant also argued that Agarwal did not teach the subsets form each register. Agarwal did not specifically show the selection of the first subset of element and the selection of the second subset of elements comprising the combination of odd, even, lower or upper as claimed. Agarwal disclosed only a combination of even and odd (see col. 13, lines 10-25). However, Cho disclosed an input odd subset of data element selection circuit (310) for selecting a first and a second data elements (see col.5, lines 11-20). It would have been obvious to one of ordinary skill in the art to use Cho in Agarwal for selecting the first and second plurality of elements as claimed because the use of Cho could increase the flexibility of loading the vector elements to accept to different order of the input vector, such as even or odd data elements, at a specific sequence of the input vectors, and it could be done by inserting a selector into the vector register interface unit of Agarwal to adaptively select the either the first or second vectors from the vector registers.

10.   As to d) , Agarwal also included 64 bits as recited in claim 54 (see the 64-bit aligned vector in col.15, lines 31-67, col.16, lines 1-16). As to the eight 8-bit and four 16-bit, Examiner holds that 64-bits is applicable to any combined length of total 64 bits. For example, 4 8 X 8 = 64, and 4 x 16 is also 64 bits. As to the starting byte in claim 57, see 32 bit in the first register , see the use of byte or word col. 15, lines 15-30. As to the contiguous locations (see the contiguous memory address in fig.4A).

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new

number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00

PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax

phone number for the organization where this application or proceeding is assigned is 703 306

5404.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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GROUP